REMARKS

The claims are claims 44, 46, 48, 52, 53 and 57 to 75.

Claims 44, 47 and 52 have been amended. New claims 57 to 75 have been added. Claims 44 and 52 have been amended to recite the external interface corresponding to transfer processor 11 is the only connection between the first and second data processors and external memory. This subject matter is illustrated in Figures 1, 2 and 17 and disclosed in the original application at page 112, lines 31 to 33. Claim 47 is amended to recite that the first read/write memory may be accessed by either processor but that the second read/write memory may only be accessed by the second processor. New claims 67 and 72 recite similar subject matter. This subject matter is illustrated in the original application at Figure 2, showing parallel processors 100 to 103 connected to internal memory 10 and master processor 12 connected to both internal memory 10 and data cache 13 via line 171. Figure 4 illustrates crossbar 20 in detail. In Figure 4: the global port of parallel processor 100 can access memory sections 10-0 and 10-2 to 10-16 and a corresponding parameter memory via horizontal 2; the global port of parallel processor 101 can access memory sections 10-0 and 10-2 to 10-16 and a corresponding parameter memory via horizontal 3; the global port of parallel processor 102 can access memory sections 10-0 and 10-2 to 10-16 and a corresponding parameter memory via horizontal 4; and the global port of parallel processor 103 can access memory sections 10-0 and 10-2 to 10-16 and a corresponding parameter memory via horizontal 5. Master processor 12 can access its own data memories, any parameter memory, data memories 10-0 and 10-2 to 10-6 via bus 171 and horizontal 1. None of parallel processors 100 to 103 can access the data memories of master processor 12. The external interface operation in response to packet requests (requests for data

movement) recited in claims 57, 60 and 63 is disclosed in the original application at page 24, lines 7 to 25 and page 112, line 30 to page 113, line 21. The limitation on indication of amount of data, source address and destination address appearing in claims 58, 61 and 65 is described in the application at page 113, lines 18 to 21. The limitation on the priority of memory access appearing in claims 59, 62, 66 and 71 is described in the application at page 25, lines 21 to 25. The limitation on instruction cache service via an external interface recited in new claim 75 is described in the application at page 78, lines 8 to 21 and page 112, line 34 to page 113, line 14.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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